Page 2

IN THE CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit device comprising:

a plurality of external signal input/output circuits;

a plurality of internal circuits arranged internally in a circuit forming region, said internal

circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said

inter-circuit signal wire is not directly connected to said external signal input/output circuits [an

input-circuit or an output circuit];

an active element in a first connection configuration connected to said inter-circuit signal

wire; and

a plurality of other active elements in a second connection configuration including

elements of an identical [or similar] structure to said [an] active element in the [a] first

connection configuration [connected to said inter-circuit signal-wire],

said plurality of active elements in the [said] second connection

configuration being arranged adjacent to said active element in the first

connection configuration to sandwich or surround said active element in the first

connection configuration,

gates of said plurality of active elements in the [said] second connection

configuration being connected only to power lines of said internal circuits

associated therewith [and being isolated from signal wires other than said inter-

circuit signal wire].

Attorney Docket No.: 052593-5003 Application No.: 09/625,643

Page 3

2. (Previously Amended) A semiconductor integrated circuit device according to claim 1,

wherein each of said internal circuits includes a plurality of basic cells regularly arranged in

repetition, and said active element in the first connection configuration and said plurality of

active elements in the second connection configuration are allocated to some of said basic cells.

3. (Original) A semiconductor integrated circuit device according to claim 1, further

comprising a substrate formed in a single chip, and said circuit forming region is allocated to one

surface of said substrate.

4. (Cancelled)

5. (Currently Amended) A semiconductor integrated circuit device comprising:

a plurality of external signal input/output circuits;

a plurality of internal circuits arranged internally in a circuit forming region, said internal

circuits having different power lines;

an inter-circuit signal wire arranged to interconnect said internal circuits, wherein said

inter-circuit signal wire is not directly connected to said external signal input/output circuits [an

input circuit or an output circuit];

an active element in a first connection configuration connected to said inter-circuit signal

wire; and

Attorney Docket No.: 052593-5003 Application No.: 09/625,643

Page 4

another [an] active element in a second connection configuration arranged adjacent to said [an] active element in the [a] first connection configuration [connected to said inter-circuit signal wire], including

an element of an identical [or similar] structure to said active element in the first connection configuration,

gates of said active element in the [a] second connection configuration being connected only to power lines of said internal circuits associated therewith [and being isolated from said inter-circuit signal wire and other signal wires].

- 6. (Original) A semiconductor integrated circuit device according to claim 5, wherein a plurality of said active elements in the second connection configuration are arranged to sandwich or surround said active element in the first connection configuration.
- 7. (Previously Amended) A semiconductor integrated circuit device according to claim 5, wherein each of said internal circuits includes a plurality of basic cells regularly arranged in repetition, and said active element in the first connection configuration and said plurality of active elements in the second connection configuration are allocated to some of said basic cells.
- 8. (Original) A semiconductor integrated circuit device according to claim 5, further comprising a substrate formed in a single chip, and said circuit forming region is allocated to one surface of said substrate.

Attorney Docket No.: 052593-5003 Application No.: 09/625,643

age 5

9. (Cancelled)

10. (Currently Amended) A semiconductor integrated circuit device according to claim 5,

further comprising an active element in a third connection configuration, arranged adjacent to

said active element in the first connection configuration and including an element of an identical

[or similar] structure to said active element in the first connection configuration, gates of said

active element in the third connection configuration being connected to a power line of an

internal circuit associated therewith and said inter-circuit signal wire and being isolated from

other signal lines].

11. (Original) A semiconductor integrated circuit device according to claim 10, wherein a

plurality of said active elements in the third connection configuration are arranged to sandwich

or surround said active element in the first connection configuration.

12-14. (Withdrawn)

15. (Previously Amended) A semiconductor integrated circuit device according to claim

10, wherein:

a plurality of said inter-circuit signal wires having different communication directions

from each other are arranged to interconnect a pair of internal circuits;

Attorney Docket No.: 052593-5003

Application No.: 09/625,643

Page 6

said active element in the second connection configuration and said active element in the

third connection configuration are arranged adjacent to said active element in the first connection

configuration on a reception side of said inter-circuit signal wire in one of said pair of internal

circuits; and

said active elements in the third connection configuration are arranged independent of

said active element in the second connection configuration, near said active element in the first

connection configuration on a reception side of said inter-circuit signal wire in the other one of

said pair of internal circuits.

16. (Previously Amended) A semiconductor integrated circuit device according to claim

15, wherein said active elements in the second connection configuration and said active elements

in the third connection configuration are arranged to sandwich or surround said active element in

the first connection configuration.

17-45. (Withdrawn)

1-WA/1992948.1